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technology: A network approach**

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STRATEGIC INTERACTIONS IN DRAM AND RISC TECHNOLOGY : A NETWORK APPROACH

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INTRODUCTION

Cooperative agreements have been ignored in business literature for a very long time. Only recently, the use of cooperative agreements as part of corporate strategies gained substantial interest. This increase in attention is above all due to the fact that in the last decade the number of cooperative agreements by firms has rocketed. In fact cooperative agreements have outnumbered the fully owned foreign subsidiaries (Contractor and Lorange, 1988). In this paper we will use the term cooperation to denote cooperative agreements between partners which are not connected through (majority) ownership. A cooperative agreement can be seen as an agreement which is positioned between two extremes, arm's length transactions on the one hand and the merger of the two firms on the other hand.

Cooperation among companies is usually analyzed in strategic management literature on the dyadic level or on the level of the participating firms. Only recently, interest by economists has grown to study cooperative efforts of firms within an inter-organisational network framework (see e.g. Hagedoorn and Schakenraad, 1990, 1992, 1993). In high-tech industries where almost all incumbents are linked to each other by means of a network of cooperative agreements, an analysis on the level of the individual players or alliances is not appropriate to understand the strategic value of cooperative strategies. In an environment which is characterised by a mix of cooperation and competition and where firms are embedded in a set of relationships, strategic action cannot be analyzed properly on the individual firm level or dyadic level. Rather it involves part or even the whole network to which the firm is linked.

Most papers on industrial networks belong to strategic management literature, and it is surprising that only a handful of articles provide a detailed statistical study of the structure and the evolution of strategic alliance (SA) networks. One way to analyze such

¹ Names of authors in alphabetic order.

networks in an empirical way is network analysis² : It will be used in this paper as statistical tool. But a statistical analysis of a network is only useful for management related issues if the results of the network analysis can be translated into and used as feedback for managerial problems *vis-à-vis* cooperative strategies.

In this paper we focus on similarities and differences between two networks of strategic alliances related to two IC technologies - the DRAM chip and RISC microprocessor. We restricted our attention to these two SA networks for three reasons. First, they can be clearly defined as an technology which leads to an identifiable product (DRAM memory chips and RISC microprocessors). Most studies on strategic alliance networks focus on industries or markets, but we prefer to highlight networks around a particular technology because technology based strategic alliances cut across industry boundaries. Second, these markets are among the few ones that have a dense network of cooperative agreements among a limited number of players - there are 43 firms in the RISC network and 72 firms in the DRAM network. The restriction on the number of players is dictated by the limited calculation capabilities of software packages for network analysis as well as by the need to restrict the number of players in order to work out a credible industry analysis that copes with cooperative strategies. Third, firms in the RISC market establish cooperative agreements for different reasons than those in the DRAM market. DRAM manufacturers are well known to team up in order to deal with the enormous R&D costs, short life cycles and steep learning curves. RISC manufacturers on the other hand are often found to be engaged into cooperative agreements in order to establish a new industry standard. By comparing both networks we might learn about the way different competitive drivers and cooperative strategies are translated into differences in network structure and in network positions of focal partners.

The paper is structured as follows. The first section describes the two technologies and the role of strategic alliances in both cases. We then proceed in a next section with the description of the data and a graphical representation of the networks by using multi-dimensional scaling techniques. The core of our empirical study is displayed in the third section. In this section we introduce various measures of centrality and apply them to both technologies. The use of these centrality measures provides us with a better understanding of the position of individual companies in the overall network. Finally, section four offers a summary and some conclusions.

² Network analysis has only recently been applied to industrial networks. For an example, see Nohria and Garcia-Pont(1991) and for a more elaborated exposition on industrial networks, see Axelsson and Easton (1992).

1. DRAM AND RISC TECHNOLOGIES

Before proceeding with the network analysis it is important to understand the role of technology related strategic alliances. Therefore, in this section, we provide a short description of the two technologies, followed by an analysis of their role in different segments of the electronics industry and the motives why companies set up strategic alliance networks.

1.1. Strategic alliances in the DRAM market

Dynamic Random Access Memories (DRAMs) are a particular general-purpose kind of memory chip, which continue to be the commodity that turns the IC industry and account for as much as a fifth of the total integrated circuit (IC) industry. Furthermore, DRAMs are in general considered as a process technology driver from which innovations can be easily diffused into other segments of the IC industry. In this way, its strategic value is much larger than its mere market share in the IC industry.

The production of DRAMs has been used as an example that highlights the dynamic relationship between innovative leads, economies of scale, learning by doing, oligopolistic exploitation of these advantages, and international competition. Strategic alliances are used frequently as a tool to accomplish one of these competitive advantages. In the following paragraphs the interaction between technological change, production volume, and vertical and horizontal diversification will be discussed. At the same time, attention will be paid to implications of these economic features for the emergence of strategic alliance networks.

1.1.1. Technological evolution

One of the key characteristics of the semiconductor industry is its *extremely rapid pace of technological change*. DRAMs are and will continue to be the IC process technology drivers for the foreseeable future. The trend towards ever increasing integration levels puts continuous pressure on processing technology requirements in the different stages of the manufacturing process. As a result, DRAM manufacturers have to spend huge amounts of money on R&D to realize these technological developments or just to follow the rapid pace of technological advances in the memory chips market. R&D budgets typically fluctuate around 15% of company sales. Forecasts predict that R&D costs (and

fabrication plant costs) will soar with each introduction of a new DRAM generation³. The escalating R&D and investment costs are one of the main reasons why DRAM manufacturers are teaming up to develop and produce future DRAM generations. Even the largest companies are now joining forces by means of international alliances⁴. Sharing the huge R&D costs and risks inherent in technological innovations becomes a necessary condition for survival.

As R&D and capital costs for new DRAM generations are increasing dramatically, only a handful producers can stay active in this market⁵. The situation is similar to that of poker players who must continuously raise the bet just to stay in the game. It is, therefore, not surprising that the monetary burden for some firms became overwhelming and that also the major DRAM manufacturers are teaming up in order to survive.

1.1.2. Dynamic-scale economies and learning effects

DRAMs are mass-produced chips used in many electronic products, and they have to be compatible with the industry standards demanded by consumers and software suppliers. Consequently, DRAMs are commodity items for which pricing strategies are extremely important as a competitive factor. Pricing of DRAMs is a complex process which depends on a set of key features of the semiconductor industry determining the cost structure.

First, the DRAM market is characterized by the *succession of different families of DRAMs*. The technological trajectory of the DRAM technology is driven by the imperative for higher reliability and performance realised by progress in miniaturization and integration. This progress materialized into a succession of new generations of DRAMs every 3 or 4 years, cannibalising the demand for the previous generation.

The shortness of the production cycle makes *dynamic-scale economies* important in two ways. First, the ever increasing R&D and capital costs cannot be amortized by cumulative production of many years, so that these sunk costs constitute a large part of the firm's cost, and average per-unit cost depends strongly on sales volume⁶. Second, the DRAM manufacturing processes are characterised by significant *learning* effects,

³ See Neff (1990).

⁴ The best example is the three-way hookup between Toshiba, IBM and Siemens to develop the 256 Mb DRAM before the end of the century.

⁵ The Nomura Research Institute (1992) calculated that three producers are enough to suffice the demand for 16Mb DRAMs.

⁶ R&D and capital costs range from 30% to 45% of DRAM sales (Mouline and Santucci (1992, p. 25)).

which are the result of potential improvements in the yield rate⁷. Since the product cycles are short, DRAM manufacturers are always in the early, steep part of the learning curve, so that average unit cost falls sharply with cumulative output. In memory chips, the highest profits come in the first year of the new chip generation when supplies are tight and demand high. "Time to market" is thus an important element for a successful strategy in this industry and it is the driving force after the recent international technological cooperative agreements between major DRAM producers. Prominent examples are the links Hitachi-Texas Instruments, AT&T-NEC, and IBM-Toshiba-Siemens.

Although the product life cycle of DRAMs is short, their development cycle is long⁸. Consequently, *processing technology* has been a major source of technology transfers agreements between technological leaders and laggards in the DRAM market. Leading Japanese DRAM manufacturers have also shared their competence in CMOS fabrication technology in exchange for design capabilities of microprocessors and other logic devices in which US firms usually excel⁹.

The race between competitors to be first in the market with the next generation of DRAMs causes periodic periods of over-production. The cyclical nature of the industry in combination with the enormous sunk costs prohibiting incumbents to exit, shapes the DRAM market into a very risky business. Dumping practices are very likely to occur during slumps as increased volume it allows to earn back part of the sunk costs and to move down along the learning curve.

1.1.3. Vertical and horizontal integration

Many electronic manufacturers invest heavily in DRAMs not because they expect the business to be a profitable one but because of strategic reasons¹⁰.

The volume production that DRAMs require, propelled them into the position of technology driver stimulating (and funding the huge depreciation costs of) the advancements in IC manufacturing technologies, that, in turn, can be applied to the production of all other ICs. The volume production of DRAMs allows a chip

7 At the introduction of new DRAM family an average yield does not surpass 15%, while most manufacturers achieve a 85% yield after 24 months (Mouline and Santucci (1992, p. 26)).

8 It can take 10 years to move a generation of chips from the development stage through volume production.

9 See Haklisch (1986) and Chesnais (1988), ICE (1993).

10 The Nomura Research institute (1992) calculated that return on investment in semiconductor operations have been less than 1% in the last four years.

manufacturer to use the latest DRAM technology for the production of other ICs, while it pulls down at the same time the unit cost of the latter. This has, of course, implications for the horizontal strategy of IC manufacturers. Methé (1991) has demonstrated that firms which produce a broader, full line of ICs are doing better. Beside these intra-firm technological spillovers between different kind of ICs, DRAM manufacturers sell other IC devices because they are less price sensitive.

Market transactions between DRAM suppliers and system producers has often been tense. Problems in the market for standard DRAMs have been alleviated by means of *(mutual) second-sourcing agreements* between IC manufacturers in order to improve market transactions between IC manufacturers and electronic system companies. The *raison d'être* of second-sourcing agreements in the DRAM market is to avoid market power exercised by a single or a few DRAM suppliers which can control industry output¹¹. They are an interesting instrument for industry leaders which like to free their human and financial resources for newer and more specialized ICs, while they assure themselves of a reliable second source.

The strategic value of DRAMs as *enabling* technology goes well beyond the semiconductor industry. Having access to the latest generation of semiconductor technology has become increasingly critical to successful competition in many businesses related to electronic systems : Although semiconductors represent only on average 7% of the value of electronic systems, most frequently they determine 100% of their performance¹². Therefore, it is not surprising that *forward and backward integration* has become an important determinant in the search for a successful strategy in this industry.

Vertical integration is becoming important for a number of reasons. First, the ever-increasing integration made it possible to place a growing number of a system's components on a single silicon chip. A decade ago, chips were standard commodity chips used as building blocks for more complex system designs, but, today, an entire system can be integrated on a single chip. The growing *convergence* between the components industry and the electronic systems industries implies that electronic system makers increasingly have to provide proprietary design information to the IC manufacturer. This need to surrender proprietary information has made vertical integration an increasingly attractive option¹³. This is particularly true when DRAM producers - or makers of other ICs - are vertically integrated and compete with their

11 See Collins and Doorley (1991).

12 See Mouline and Santucci (1992).

13 See Flamm (1990 p. 229).

customers in electronic systems industries ; In this case DRAM manufacturers have an incentive to cut or to retard supply their chips or to postpone the supply of their latest IC technology.

Backward connection into in the semiconductor equipment market and the semiconductor materials market is also important¹⁴. Because DRAMs are process technology drivers, close connection with these two upstream markets yields information resources needed to cope with technological challenges in the different production stages of a new DRAM family. The ability to interact in a cooperative fashion with suppliers of key subtechnologies and to share information with them has become more important as DRAMs became more sophisticated devices¹⁵.

In short, we can conclude that strategic alliances in the DRAM market are *not directly* influencing the competitive position of DRAM manufacturers. The link is always *indirect* : strategic alliances are established in order to improve the technological position of the partners, which, in turn, is likely to improve their competitive position. In the next section, we focus on the SA network around the RISC-microprocessor technology, where companies try to improve their competitive position directly by means of cooperative agreements.

1.2. Strategic alliances in the RISC microprocessor market

RISC microprocessors are relatively new and are a mounting threat for established industry standards in the PC market; Intel based CISC chip designs are said to be slower than new RISC architectures and the MS-DOS operation system may face competition from the Unix operating system (OS), which is till now a common OS for RISC based workstations. The quest to establish new standards is one of the main reasons for RISC designing companies to team up with other companies. Since the RISC microprocessor technology became popular in the late eighties, a thickening web of strategic alliances, joint ventures, technology-licensing deals and consortiums has been established between IC manufacturers, computer makers and software writers.

14 The semiconductor equipment industry includes wafer fab, assembly and test equipment. The semiconductor materials industry includes chemical and gases, packaging materials, wafers and photomasks.

15 The advantages of vertical integration have nevertheless been criticized the last years because of the apparent success of fabless firms and of some non-integrated specialized DRAM manufacturers as Micron Technology Inc. If a fabless strategy is a sustainable one remains an open question. The success of some specialized IC and DRAM manufacturers highlights that specialization generates benefits, which have to be traded off against those emerging from vertical integration.

In order to evaluate RISC microprocessor technology, we specify RISC architectures and their role in microprocessor and computer markets in the next section. Subsequently, we investigate the impact of an industry standard regarding to the RISC technology on the microprocessor and computer markets¹⁶. Special attention will be paid to the interaction between these markets and to the relation between the search for a new industry standard and the establishment of SAs. In a last subsection, some conclusions are drawn and hypotheses formulated regarding to the emergence of the SAs network *vis-à-vis* the RISC technology.

1.2.1. Risc-microprocessor architectures

RISC microprocessors deliver significant cost/performance advantages over computers based on the traditional CISC (Complex Instruction Set Computer) microprocessors. In the traditional CISC approach designers brought all the instructions into the central processor itself, minimising in that way memory requirements. RISC architectures stress the reduction and simplification of the instruction set in order to obtain the highest performance possible from available technology. The leap in performance *vis-à-vis* CISC is based on a more sophisticated division of complexity between hardware and software : RISC chips dispense with all but the most commonly used instructions - about 20% of the total.

The technical characteristics of RISC designs can be translated in economic benefits *vis-à-vis* CISC designs. Reduced and simplified instructions mean simpler circuits that need fewer transistors. Besides the fact that the relatively small and simple control unit in the RISC design makes the microprocessor faster, it also implies a reduction in the overall design costs and design time, reducing the probability that the end product will be obsolete by the time the design is completed. At the same time, the number of design errors decreases and therefore reliability improves. Moreover, it is easier to locate and correct those errors¹⁷.

¹⁶ We made abstraction of the implications of the introduction of RISC-microprocessors on the software market in order to shorten the paper.

¹⁷ It takes usually three or four years before a new family of CISC microprocessors hits the market. Flaws in the samples of CISC designed microprocessors can delay time to market from a few months up to half a year. See Johnstone (1991).

1.2.2. The quest for an industry standard: The microprocessor and computer markets

The RISC microprocessor market is characterized by a network of strategic alliances, joint ventures, and technology-licensing deals. In order to analyze these networks it is important to understand how RISC designs can play a role in fulfilling computing requirements of customers. Two points have to be analyzed in more detail. First, microprocessors are only one core component in computers which are always sold as a package or bundle of hardware and software. Sales of computers not only depend on their cost/performance ratio but also on the existence of an industry standard or "open" system software. Second, RISC architecture, which is mainly used in the workstation market, is considered to be a technology that can easily penetrate other computer segments in the future ; On the one hand, it can take over the minicomputer and mainframe computer markets by networking, and, on the other hand, it can penetrate the PC market through low cost offerings.

In order to understand why computer manufacturers, software writers and companies with a proprietary RISC architecture are eager to get control over the RISC-based computer markets, we have to look at the requirements for competitive success in the information technology industry in general and the computer industry in particular. In almost all cases, architectures in open systems are proprietary¹⁸ and they generate huge profits for a small handful of companies that supply components defining and controlling the critical functions of the computer or electronic system. Typical architectural standard setters are microprocessor designers (Sun and MIPS in RISC, Intel in CISC), and operating system vendors (Sun's or IBM's version of UNIX and Microsoft's DOS or Windows NT). While most microprocessor and computer manufacturers have a hard time, firms that control such critical architectural control points, as the system software and the microprocessor design, have generous after-tax margins.

Because RISC-microprocessor technology represents an alternative to the established PC standard, it has the potential to shake up the computer industry. Many IT companies are developing (cooperative) strategies *vis-à-vis* the emergence of the RISC technology, since the latter is expected to change their competitive position in the future. We will discuss these strategies in different steps. First, we focus on the microprocessor market,

¹⁸ It is fallacious to think that in open systems proprietary architecture control is no longer possible or desirable. Morris and Ferguson (1993, p. 89) argue that the opposite is true, as architectural coherence becomes even more important in an open systems era and non-proprietary system architectures have proven to be static and unable to keep up with rapid technological changes. Proprietary architectures, by contrast, are under constant competitive attack and must be vigorously defended. This dynamic compels a very a rapid pace of technological improvement.

followed by the implications for the computer industry. Subsequently, attention will be paid to the battle for dominance between different operating systems. Finally, conclusions will be drawn with respect to the cooperative strategies and the SA network associated with RISC technology.

1.2.2.1. *Competing RISC designs*

Commercial RISC designs began to appear in the late eighties and RISC chips are still used primarily in workstations, which are only a fraction of the computer industry¹⁹. But RISC chips have an excellent growth potential because workstations constitute the fastest growing sector of the computer market. Moreover, RISC based computers tend to penetrate a whole range of submarkets in the computer industry ; On the one hand, flexible workstation networks based on multiple microprocessors are making inroads into minicomputers and mainframes, as workstations built from RISC chips can perform the same computation work for a fraction of what it would cost with a mainframe computer. On the other hand, further price reductions for RISC chips will open the huge personal computer market²⁰.

Consequently, it is not surprising that economic players from outside the workstation and RISC chip markets are interested in RISC architectures. In 1992, several RISC designs competed for market share (see table in annex B). Since RISC chips have the potential to be used in a wide range of computers, the emergence of an industry standard for RISC microprocessors could eventually supplant the aging PC standard, which is based on Intel Corp. CISC chips. Firms with a proprietary RISC architecture are now aggressively promoting their architecture by means of *free licensing and other cooperative agreements*.

The establishment of a new industry standard creates positive network externalities and generates benefits for computer users, RISC manufacturers, and RISC-based computer makers. The adoption of a compatible RISC designs speeds up volume production and brings down prices. Without compatible RISC designs, users are likely to stick to the PC standard which incorporates an inferior technology.

¹⁹ According to Dataquest Inc. 387,000 RISC chips were sold in 1990 by all manufacturers, whereas Intel Corp.'s 386 and 486 CISC chips, used in the PC market, totalled 7.5 million in unit sales.

²⁰ NEC intends to introduce in 1993 a RISC processor aimed at the PC market and the Apple/IBM/Motorola alliance (see infra) will use RISC processors in their PC systems in the mid-90's. Similarly TI and Sun Microsystems are developing the microSparc microprocessor targeting workstation performance at PC prices. See Johnstone (1992), ICE (1993), Halper (1992), Valigra (1992), and Kupfer (1992).

Two early movers in the RISC market were workstation sellers MIPS Computer Systems Inc. and its larger rival Sun Microsystems Inc.. They pushed hard for clones to get their architecture as the basis for a new industry standard. Sun's strategy is to license freely the design of its SPARC microprocessor inviting other companies to clone its machines. Such licensing agreements are interesting for all agents involved. It increases the probability of SPARC to become an industry standard, which creates a growing market pie and thus offsets the negative effects of increased competition between Sun and its clone makers²¹. The latter get access to the technology and multiple license agreements operate at the same time as second sourcing agreements which avoid single-supplier domination and reduces the risk of chip shortages when demand suddenly boosts. But Sun, with its 29% of the workstation market in 1991, is considered to be too large and too aggressive a competitor for top computer makers to feel comfortable cloning the SPARC design. The same competitive considerations also limit clones of IBM and H-P designs (H-P had a 19% market share of the workstation market in 1991). Intel and Motorola (the numbers 1 and 2 in conventional microchips) did not build much of a following for their RISC chips, because such efforts would cannibalize their sales of CISC chips.

MIPS Computer System Inc. with its tiny computer business seems to be neutral to establish a standard. In order to slow the acceptance of Sun's SPARC architecture, MIPS and Compaq spearheaded the formation of a group of 21 companies called ACE (Advanced Computer Environment). ACE members included MIPS, Compaq, DEC, NEC, Microsoft, Acer, CDC, Olivetti, Prime, Pyramid, Siemens/Nixdorf, Bull, Silicon Graphics, Sony, Sumitomo, Tandem, Wang, Zenith Data Systems, and numerous other companies. The ACE systems would use the MIPS 64-bit RISC microprocessor (R4000) as the heart of the systems. But many things went wrong since ACE began in late 1990 and the ACE consortium lost cohesiveness. In the end, MIPS lost its neutrality when it agreed to a buyout by workstation maker Silicon Graphic Inc²².

These aggressive strategies of both companies triggered reactions from the other players with a proprietary RISC design. Hewlett-Packard formed PRO, the Precision RISC Organization, to promote and coordinate the use of its PA-RISC architecture by means of developing standards for hardware and software. IBM and Motorola, who both have their own RISC architecture, joined forces to develop the PowerPC which will power a range of

21 Other industry experts, however, note that Sun and MIPS could get eclipsed by clone makers as Fujitsu, Mitsubishi and Matsushita which could eventually undercut prices. These clone makers are large diversified firms, which can easily cross-subsidize their RISC-based computers. See Ruhl (1988).

22 See ICE (1993), and Hof (1992b).

products from notebooks to supercomputers. The venture between Apple, IBM, and Motorola is a hedging strategy of Apple and IBM against the growing threat of RISC chips for the PC market. Given the market share of both firms in the PC market (and of IBM in the mainframe market), the venture catapults them into a market position from which they have a grip on the development of a new industry standard²³. DEC was late in developing its own Alpha RISC chip, and it still has to look for partners to promote and coordinate the use of its architecture.

The growth of the workstation market and the attempts to standardize RISC architectures are indeed threatening the comfortable position of Intel Corp in the CISC based microprocessor market²⁴. If RISC-based workstations become more popular and penetrate the PC market (as well as the minicomputer and mainframe markets), RISC chip producers may become serious challengers of Intel. Although Intel produces its own i860 RISC chips, its main answer of the mounting RISC-chip threat consisted of speeding up the introduction of new families CISC based microprocessors. The workstation market is only about one-tenth the size of the PC market and is thus not important for Intel's sales figures. However, it is an important market in the strategic sense, because there is always a threat that RISC chips make an incursion in the PC market : The stronger Intel is in workstations, the less of a threat that is. The future market position of Intel Corp. depends on the relative performance of its future CISC families *vis-à-vis* that of future RISC microprocessors²⁵.

1.2.2.2. Competing for computer market share

Till now, no RISC chip has established itself as a new standard and it is unlikely that one will in the foreseeable future. It is beyond doubt that the market cannot support so many companies competing to establish a new industry standard. A growing number of alliances and shifting of strategic positions is likely to occur in the following years in order to impose own standards as the industry standard²⁶.

The fact that there is no industry leader that could impose its design as an industry standard implies that firms with proprietary RISC architectures have licensed their technology freely in order to develop an "installed base" which, in turn, can give them a

²³ See ICE (1993), Watson (1992).

²⁴ Intel has also to cope with increasing competition from clone makers as AMD, Chips & Technologies and Cyrix which are taking away market share from the lucrative 32-bit market.

²⁵ See Rice (1992), Hof (1992a), and Port (1992a; 1992b).

²⁶ For now, the Apple/IBM/Motorola alliance has the best chances to impose itself as a new industry standard and the PowerPC may be the only processor family that can give Intel a serious challenge in the PC market.

competitive advantage over their rivals. As a result, the competition for market share in the computer industry is a *direct* consequence of the competition for dominance in the RISC chip market. This competition for market share took first place in the workstation market, but it is shifting towards other segments of the computer industry as the popularity and capabilities of RISC microprocessors is growing. The table in annex C shows how different microprocessor manufacturers have to get the commitment of a number of workstations manufacturers in order to have a substantial market share.

These competitive pressures have led to even more strategic alliances and (international) equity investments among computer manufacturers. Especially financially troubled firms with an installed base are attractive partners. Recent deals between IBM and Groupe Bull, DEC and Olivetti and the acquisitions of Hal (US) and ICL (UK) by Fujitsu Microelectronics Inc., Apricot Computers PLC (UK) by Mitsubishi Electric Corp., and Nixdorf (Germany) by Siemens are the direct outcome of a switch of the industry towards open systems and flexible networks of which RISC chips may become an essential part²⁷.

In short, cooperative strategies by players involved in the young RISC technology are largely determined by the search for compatible RISC-architectures. Since there is no industry leader who could impose its RISC-architecture as an industry standard, different companies with competing architectures establish a network of strategic alliances (mainly (cross-)licensing agreements and consortiums) with IC manufacturers, computer makers and software writers to ensure their customer base. The result is that the firms involved in RISC-technology are grouped into 'strategic blocks' around the different proprietary RISC architectures. The block with the largest (combined) consumer base has the best chance to impose its RISC-architecture as the industry standard in the future.

Since the relation between strategic alliances and competition for market share in the workstation market is a *direct* one, we expect that focal partners in the SA network in the RISC market will have a relatively tight grip on the SA network. This is in contrast with the DRAM-network where the link between SAs and market share is only a *indirect* one so that the search for a dominant position in the network is less compelling.

27 See Levine (1992a; 1992b; 1992c), Nash (1992), McWilliams (1992a; 1992b; 1992c), Comerford (1992), Guterl (1990), Berkman (1990), and Verity (1992).

We expect that the nature of the linkage between cooperative agreements and market share competition has some implications for the structure of the strategic alliance network. That is the research topic of the second and third section.

2. DATA AND GRAPHICAL REPRESENTATION

2.1. The data

The data about cooperative agreements related to the RISC and the DRAM technology are extracted from the MERIT-CATI database. This database contains information on nearly 10,000 cooperative agreements involving some 3,500 different parent companies active in biotechnology, information technology new materials technology or other "non-core" technologies.

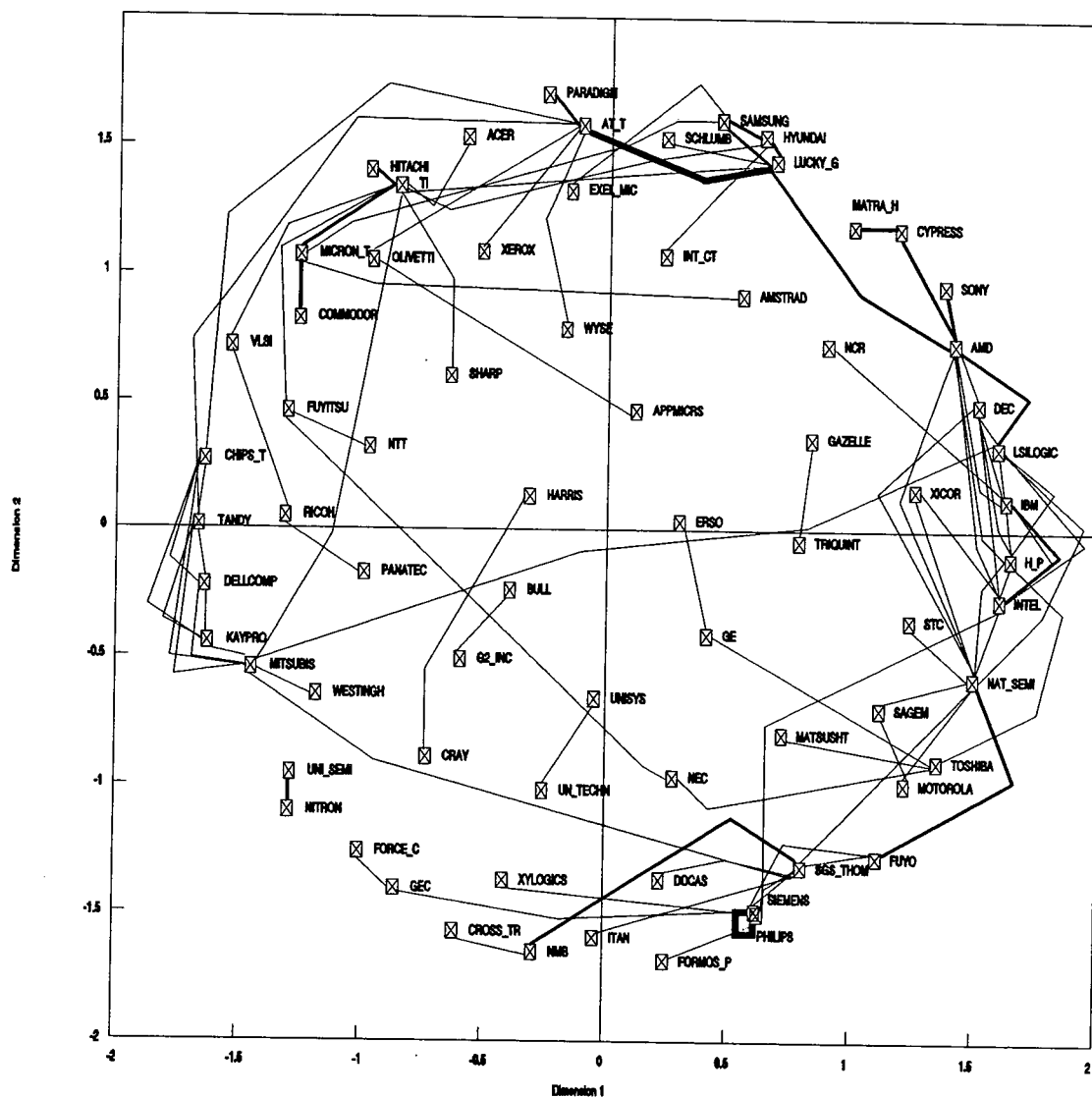
The cooperative agreements included in this network analysis all started between 1980 and 1989²⁸. The eighties have been a turbulent period for cooperative agreements in the DRAM market and the RISC technology only took off after 1985. The CATI data bank is not upgraded in a systematic way for alliances that were undertaken after 1989. Therefore, the study does not pretend to describe the actual situation in both markets. But a careful analysis of the networks in 1989 may provide us some keys why the networks evolved in the way they did in the early nineties. The data sets for the following network analysis are valued graphs where the cells of the matrices represent the frequency of a (specified kind) of cooperative agreements between two actors. However, some network procedures require binary and/or symmetric data.

2.2. A graphical representation of the networks

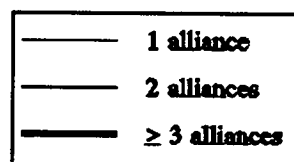
The best way to get an overview on the two cooperative networks is to draw them on two dimensional multidimensional scaling scatterplot as has been done in the following two

28 Alliances in the networks under study are composed of different forms of cooperation. In the CATI database we discriminate among seven basic forms of cooperative agreements. (a) The category 'Joint R&D' which embraces both joint research pacts and joint development agreements. (b) 'Customer-supplier relationships' which include R&D contracts, co-production contracts, co-makership contracts and customer-supplier partnerships. (c) 'Technological exchange agreements' (two directional) which include technology sharing, mutual second-sourcing and cross-licensing. (d) 'One directional technology flow' agreements consist of licensing and second-sourcing agreements. (e) 'Standardization and bidding consortia'. Equity agreements include (f) 'equity joint ventures' which enclose both the classical joint ventures as well as the research corporations', and finally (g) 'equity ownership'

Figure 2. : All cooperative agreements in the DRAM market: 1980-1989



Legend :



The two graphs reveal both similarities and differences. Both show that all firms - with the exception of a few pairwise isolates - are linked to each other in a direct or indirect way. The positions of the companies in a network form the base for their strategic action. Within a network, the position of an actor changes all the time, not only because of its own actions, but also because its counterparts' positions and those of third parties, with whom an actor has no direct relationships, are changing³⁰. Although the two cooperative networks are industry-wide, they are still sparse ; the density of the adjacency matrix that simultaneously accounts for all ties among the actors is 0.087 for the RISC market and 0.043 for the DRAM market. That is a general characteristic of industrial networks and can in part be explained by the exclusiveness of many cooperation deals and the relative inefficiency - at least in the micro-electronics industry - of consortia including many actors³¹.

The two networks are structured differently. The RISC network is clearly build around three focal players. The two major ones are the two arch rivals MIPS Computer Systems and Sun Microsystems. Hewlett-Packard seems to represent the focal actor of a third but smaller cluster of firms. The DRAM network is more like a "chain" linking most companies one by one. Although it is less obvious than in the RISC market, there exist a number of subgroups in the network ; the group around the European big three Siemens, Philips and SGS-Thomson, the US Memories Consortium including the major American companies, Texas Instruments (and AT&T) with its South-Korean and Japanese partners, and, finally the group including Mitsubishi. Mitsubishi and Intel developed cooperative agreements that cut across the whole network, which gives them freedom of action since they are not locked-in within one of the subgroups.

It is also important to mention the existence of several consortia which determine to a considerable extent the shape of the network in both markets. There were three consortia in the RISC market during the late eighties; (a) the Sparc Vendor Council³², (b) the Systems Performance Evaluation Cooperation (SPEC)³³, and the 88-Open³⁴. They were established primarily to establish industry standards and to increase compatibility between allies but also between rivals.

30 Axelsson and Easton (1992, p. 213).

31 See Boulton et al. (1992); Burrows (1992); Dinneen (1988); OECD (1991); Vickery (1992).

32 The Sparc Vendor Council includes Bipolar, FUJITSU, LSI Logic, Texas Instruments, Cypress, Matsushita and Philips. All these firms have licensing agreements with Sun Microsystems for its SPARC technology.

33 SPEC intended to develop industry-wide standard benchmarks for (32-bits) RISC architecture computers. It includes the major companies - Sun Microsystems, MIPS Computer Systems, Apollo and Hewlett-Packard.

34 The 88-Open Consortium is a consortium of computer suppliers supporting Motorola's 88000 RISC processors. It includes Motorola, Unisoft, Apollo, Hewlett-Packard, NCR, Tektronix and Data General, and it intends to foster source compatibility for the 88000 RISC processors.

The consortia in the DRAM market are mostly joint development agreements. In the early eighties NTT, Fujitsu and NEC had agreements to develop the 128 Kb and the 256 Kb DRAM chip. Similar agreements existed between Samsung, Hyundai and Lucky Goldstar in the late eighties in order to develop the 4 Mb and 16 Mb DRAM chip. There were also consortia between American DRAM producers: One of them was US Memories³⁵ which was established in 1989, but was broken up a year later. Another U.S. consortium is Sematech which tries to improve semiconductor manufacturing technologies. Since Sematech is directed towards semiconductor equipment industry instead of the DRAM market itself, it is not included in the DRAM SA network.

3. CENTRALITY MEASURES

In this section, different measures of point centrality and graph centrality are shown and discussed for both markets. An examination of the point centralities should give us an idea of the position of each partner with respect to the overall structure of the network. A comparison of these centrality measures between the RISC and the DRAM SA networks is likely to highlight differences in the value and strategic use of alliances.

3.1. Point centrality and graph centrality measures

Point centrality can be measured in several way³⁶. A first indicator (C_D) measures point centrality as a function of the degree of a point³⁷ - the mathematical formulas for the centrality measures are shown in annex A. A second, the closeness-based point centrality (C_C), measures the centrality of a point by summing the geodesic distances from that point to all other points in the graph³⁸. Another centrality measure, the so called betweenness centrality (C_B), is based upon the frequency with which a point falls between pairs of other points on geodesic paths connecting them³⁹.

For valued graphs, there also exists a centrality measure based upon maximal flow betweenness (C_F) ; The information flow between two points is not the direct flow between

35 US Memories included IBM, Hewlett-Packard, DEC, Intel, National Semiconductor, AMD and LSI Logic.

36 We confine our attention to a few centrality measures. Centrality measures based on eigenvectors as has been developed by Bonacich (1972) and the Stephenson and Zelen (1989) information centrality measure are left out of the following analysis.

37 The *degree* of a point, p_i , is the count of the number of other points, p_j ($i \neq j$), to which it is adjacent and with which it is, therefore, in direct contact (Freeman (1979, p. 219).

38 The geodesic is the shortest path linking a given pair of points.

39 Degree centrality can handle both symmetric and asymmetric valued graphs. In this section we treat a matrix in a symmetric way, but this will change when we examine in and outdegrees. Closeness centrality is always based on symmetric binary graphs, while betweenness centrality can handle both symmetric and asymmetric binary graphs. Flow betweenness works with valued graphs and the Bonacich's power with symmetric binary graphs (these indicators are explained in the following paragraphs).

adjacent points but the overall flow between pairs of points along all the paths that connect them. As a result, the information flow between two points depends on the capacity of all the channels of communication on all the paths that connect them. A channel, in its turn, is defined as the value of the connection linking two points and it determines the capacity or the maximum amount of information that can be passed between both⁴⁰.

A last measure of point centrality, C_p , is based on the Bonacich power index. The measure is generated by two parameters, α and β . The value of α is used to normalize the centrality measure. The parameter β reflects the degree to which an actor's status is a function of the statuses of those to whom he is connected to. If β is positive, C_p is a conventional centrality measure in which each company's status is a positive function of those it is linked to in the strategic alliance network ; This may be the case in technology exchange or joint ventures, where it is favourable to be connected to powerful partners. However, if β is negative, power comes from being connected to those who are powerless. These types of situations prevail when bargaining power is important - supplier/consumer relationships and equity investment links are likely to be characterized as such. If $\beta=0$, C_p is simply proportional to the degree of a company, i.e. the number of partners it is connected to, regardless of their centralities⁴¹.

Graph centralisation or the centrality of an entire network measures the tendency of a single point to be more central than all other points in the network. As a consequence, graph centrality measures are based on differences in point centralities, and more precisely, on the difference between the centrality of the most central point and that of all others (Freeman (1979, p. 227) - see formula (A.10) in annex A. There are as many graph centrality indices as there are point-bases and they all assign the highest centrality index to the 'star' or 'wheel' network structure, in which one point is connected with all other, while the latter have only one edge with the former. The lowest scores appear for a complete graph and the circle. But beyond these extreme cases, agreement between the graph centralisation indices breaks down.

⁴⁰ For further details on this centrality measure, see Freeman *et al.* (1991).

⁴¹ The measure is appropriate for both symmetric and asymmetric relations. If there are asymmetric relations, the Bonacich power based centrality with $b>0$ measures prestige, and, if the relations are symmetric, it measures centrality.

3.1. Centrality in the RISC network

The point and graph centrality measures of the strategic alliances network in the RISC market are represented in table 1. These measures are relative or normalized measures, so that comparison between the RISC and DRAM SA network is straightforward.

Table 1 : Point and network centrality measures for the RISC microprocessors

Company	C_D	C_C	C_B	C_F	C_P $b=-0.05$	C_P $b=0.05$
SUN_MICR	61.90	18.10	25.53	30.90	14.80	25.99
MIPS_CS	42.86	18.03	18.35	36.58	14.13	20.95
H_P	26.19	17.57	12.22	24.22	7.04	15.68
TI	23.81	16.15	2.57	6.19	5.73	13.29
APOLLO	21.43	17.43	6.51	11.86	5.04	13.53
LSILOGIC	21.43	16.87	1.63	2.15	5.04	14.11
PHILIPS	21.43	16.15	2.45	9.92	5.71	13.27
BIPOLAR	19.05	16.09	1.12	1.99	4.73	12.16
CYPRESS	19.05	16.09	0.02	1.52	4.73	12.16
FUJITSU	19.05	16.09	0.02	1.14	4.73	12.16
MATSUSHT	19.05	16.09	0.02	1.40	4.73	12.16
MOTOROLA	16.67	15.61	1.34	2.46	5.47	10.41
DATA_GEN	14.29	15.56	0.00	1.42	4.45	9.39
NCR	14.29	15.56	0.00	1.42	4.45	9.39
TEKTRONX	14.29	15.56	0.00	1.42	4.45	9.39
UNISOFT	14.29	15.56	0.00	1.42	4.45	9.39
PRIME	4.76	16.41	0.00	0.00	0.55	4.35
CDC	4.76	15.97	0.76	2.98	1.01	3.71
AMD	4.76	15.67	0.51	6.78	1.36	3.45
NEC	4.76	15.67	0.00	0.00	1.25	3.11
UNISYS	4.76	15.61	0.00	0.00	0.26	2.30
XEROX	4.76	15.61	0.00	0.00	0.26	2.30
DEC	4.76	15.56	0.00	0.00	0.29	2.05
KOBUTA	4.76	15.56	0.00	0.00	0.29	2.05
ARETE	2.38	15.61	0.00	0.00	0.26	2.30
AT_T	2.38	15.61	0.00	0.00	0.26	2.30
LUCKY G	2.38	15.61	0.00	0.00	0.26	2.30
METAFLOW	2.38	15.61	0.00	0.00	0.26	2.30
TOSHIBA	2.38	15.61	0.00	0.00	0.26	2.30
INTEG DT	2.38	15.56	0.00	0.00	0.29	2.05
PERF SEM	2.38	15.56	0.00	0.00	0.29	2.05
RACAL	2.38	15.56	0.00	0.00	0.29	2.05
SIEMENS	2.38	15.56	0.00	0.00	0.29	2.05
SILICONG	2.38	15.56	0.00	0.00	0.29	2.05
STARDENT	2.38	15.56	0.00	0.00	0.29	2.05
TANDEM	2.38	15.56	0.00	0.00	0.29	2.05
HITACHI	2.38	15.22	0.00	0.00	0.65	1.78
SODIMA	2.38	13.77	0.00	0.00	0.94	1.16
SGS/THOMS	2.38	13.73	0.00	0.00	0.73	1.52
INTERGRA	2.38	2.38	0.00	0.00	0.95	1.05
OLIVETTI	2.38	2.38	0.00	0.00	0.95	1.05
SCHLUMB	2.38	2.38	0.00	0.00	0.95	1.05
VLSI	2.38	2.38	0.00	0.00	0.95	1.05
Mean	10.52	14.60	1.70	3.39	2.66	6.31
Std	12.18	4.00	5.00	7.99	3.38	6.06
Network Centralisation	53.89	7.26	24.40	33.98	12.43	20.15

The simplest conception of point centrality is C_D , the centrality as a function of the degree of a point. A point with a high C_D -value is considered to be "in the thick of things", so that in some sense it is a focal point playing an essential role in the network. A point with a low degree is isolated from most other actors in the network and will only play a marginal role. The 2 firms with high degree centrality are MIPS Computer Systems Inc. and Sun Microsystems Inc. Their focal position is the result of their active policy of RISC-architecture licensing. Other firms with a relatively high C_D -value are Hewlett-Packard, who acquired Apollo in 1990, Texas Instruments, LSI Logic and Philips. The last three companies belong to the "cluster" of firms that have a licensing agreement with Sun Microsystems : The high ranking of these firms is an indication of the network density of that "cluster". Hewlett-Packard/Apollo, on the contrary, is the focal partner of a group of firms that constitute a third cluster beside those of MIPS Computer Systems and Sun Microsystems. At the lower part of table 2, a range of firms have only one (2.38%) or two (4.56%) strategic alliances and are marginal players in the network analysis.

The second column in table 1 represents the closeness-based index : centrality of a point is measured by summing the geodesic distances from that point to all other points in a graph. Again, MIPS Computer Systems, Sun Microsystems, and Hewlett-Packard have the highest closeness centralities but their value is of the same order of that of other companies. That implies that the RISC alliance network exhibits a number of loops or circles: The central loop is the triangle between Sun, MIPS and H-P, but also other companies have direct links to companies in another cluster. The result is that the variance of the distance of the geodesics across the firms is relatively small. Translated in strategic terms, this means that companies are never far away from the "center" of the network. Exceptions are Olivetti, Schlumberger, VLSI and Intergraph, which have an extremely low value for this indicator, as their alliances are isolated from the main network.

The betweenness centrality index is based on the frequency with which a company falls between pairs of other companies on the geodesic path between them. A firm that falls on the shortest path between two other firms has a potential for control. Sun Microsystems, MIPS Computer Systems and Hewlett-Packard have a clear potential for such control. Their value is even higher for C_F , i.e. when we take all paths into account,

which, in its turn, confirms the presence of cycles in the network⁴². Some firms have bridge functions, such as CDC and LSI-Logic between MIPS Computer Systems and Sun Microsystems, AMD and Philips between Sun Microsystems and Hewlett-Packard, and Motorola between Hewlett-Packard and Thomson.

The ranking is more or less the same for the Bonacich's power based centrality measure. If β was equal to zero, the centrality measure would be directly proportional to the degree of each firm. We measured C_P twice, once with a negative (-0.05) and another time with a positive (0.05) value for β ⁴³. A comparison between both columns allows us to reveal whether a company is connected to powerful firms (in terms of strategic alliances) or to low powered companies. MIPS Computer Systems has about the same C_P level as Sun Microsystems when weight is given to being connected to low powered firms, but lags with 5% when connections with powerful actors gets more weight. This change in position between the two firms is the result of the relative high point centrality of the firms to whom Sun Microsystems is connected to *vis-à-vis* the relatively low centrality value of most partners of MIPS Computer Systems. The same argument could be provided for the relative better position of Hewlett-Packard *vis-à-vis* MIPS Computer Systems when β is positive. However, one should keep in mind that power is defined here in terms of the number and strength of alliances, so that (dis)advantages of connections with powerful or less powered partners cannot be directly translated in terms of competitive strategies. Nevertheless, the different centrality measures provide a first overview of the network positions of the different companies.

3.2. Centrality in the DRAM network

The same centrality indices are calculated for the DRAM market. They are shown in table 2 and will be discussed in comparison with the figures in table 1.

42 Connected graphs without cycles have only one path - a single geodesic - linking any pair of points. When there are no alternate paths, the counts tabulated by the betweenness measures must equal the flows of the flow-based measures. However, when cycles are present C_F and C_B will differ. That is because the C_B measures record flow only along geodesics, while the C_F measures are responsive to *all* paths along which information can flow. Therefore, the two kinds of measures will produce different results for any graph that contains any cycles." (Freeman et al. (1991, p. 150-151))

43 Larger absolute values for b polarize centrality values even more.

Table 3 : Point and network centrality measures for the DRAM market

Company	C_D	C_C	C_B	C_F	C_P $b=-0.05$	C_P $b=0.05$
AMD	18.31	8.05	11.31	33.52	6.94	13.24
TI	18.31	8.04	8.76	8.18	8.66	12.40
NAT_SEMI	16.90	7.92	10.08	12.16	8.72	15.70
LUCKY_G	15.49	8.00	12.49	16.49	4.52	8.38
AT&T	14.08	7.73	13.38	26.37	6.20	8.44
SIEMENS	14.08	7.73	6.79	10.71	5.00	7.69
LSILOGIC	12.68	8.05	14.61	9.79	5.60	12.65
SGS_THOM	12.68	8.03	11.89	15.11	6.60	10.52
INTEL	12.68	7.87	4.81	5.66	6.04	12.03
MITSUBIS	11.27	8.17	20.11	25.53	6.22	11.10
IBM	11.27	7.82	2.03	3.51	5.15	10.81
TOSHIBA	11.27	7.80	10.00	12.40	5.92	9.13
PHILIPS	11.27	7.73	3.47	4.70	3.08	5.58
H_P	9.86	7.91	2.31	1.37	4.87	11.17
SAMSUNG	9.86	7.77	2.30	2.74	3.98	6.63
DEC	8.45	7.81	0.00	0.82	4.13	9.78
HYUNDAI	8.45	7.74	1.01	2.26	3.10	5.43
MICRON_T	8.45	7.58	2.47	3.24	3.28	5.08
TANDY	7.04	7.79	3.82	0.43	3.87	6.87
CHIPS_T	7.04	7.79	5.09	5.77	3.87	6.87
FUYO	5.63	7.73	1.25	2.12	1.98	4.70
KAYPRO	5.63	7.72	0.00	0.32	3.14	5.52
DELLCOMP	5.63	7.72	0.00	0.32	3.14	5.52
MOTOROLA	5.63	7.58	0.71	2.54	2.20	4.39
CYPRESS	5.63	7.55	2.03	3.17	1.61	2.72
FUJITSU	4.23	7.69	2.62	2.28	2.44	3.81
NMB	4.23	7.54	2.03	2.79	1.62	2.58
HITACHI	4.23	7.53	0.00	0.00	0.57	1.62
NEC	2.82	7.63	4.03	4.61	1.58	2.65
VLSI	2.82	7.56	2.54	4.62	1.47	2.73
SONY	2.82	7.54	0.00	0.00	0.65	1.66
SAGEM	2.82	7.49	0.00	1.18	1.45	3.00
GE	2.82	7.33	1.09	0.57	1.66	2.51
GEC	2.82	7.27	2.03	2.59	1.70	2.44
OLIVETTI	2.82	7.27	1.07	0.74	1.64	2.48
PARADIGM	2.82	7.26	0.00	0.00	0.69	1.42
RICOH	2.82	7.12	1.31	2.38	1.88	2.19
COMMODOR	2.82	7.12	0.00	0.00	0.84	1.25
MATRA_MHS	2.82	7.10	0.00	0.00	0.92	1.14
NITRON	2.82	1.41	0.00	0.00	0.95	1.05
UNI_SEMI	2.82	1.41	0.00	0.00	0.95	1.05

Table 3 : Continued

Company	C_D	C_C	C_B	C_F	C_P $b=-0.05$	C_P $b=0.05$
WESTINGH	1.41	7.64	0.00	0.00	0.69	1.55
ACER	1.41	7.53	0.00	0.00	0.57	1.62
SHARP	1.41	7.53	0.00	0.00	0.57	1.62
ITAN	1.41	7.52	0.00	0.00	0.67	1.53
DOCAS	1.41	7.52	0.00	0.00	0.67	1.53
SCHLUMB	1.41	7.50	0.00	0.00	0.77	1.42
STC	1.41	7.43	0.00	0.00	0.56	1.79
XICOR	1.41	7.38	0.00	0.00	0.70	1.60
NCR	1.41	7.33	0.00	0.00	0.74	1.54
MATSUSHT	1.41	7.32	0.00	0.00	0.70	1.46
EXEL_MIC	1.41	7.29	0.00	0.00	0.80	1.33
INT_CT	1.41	7.27	0.00	0.00	0.85	1.27
WYSE	1.41	7.26	0.00	0.00	0.69	1.42
XEROX	1.41	7.26	0.00	0.00	0.69	1.42
FORMOS_P	1.41	7.26	0.00	0.00	0.85	1.28
XYLOGICS	1.41	7.26	0.00	0.00	0.75	1.38
NTT	1.41	7.22	0.00	0.00	0.88	1.19
AMSTRAD	1.41	7.12	0.00	0.00	0.84	1.25
CROSS_TR	1.41	7.09	0.00	0.00	0.92	1.13
ERSO	1.41	6.91	0.00	0.00	0.92	1.13
FORCE_C	1.41	6.85	0.00	0.00	0.91	1.12
APPMICRS	1.41	6.85	0.00	0.00	0.92	1.12
PANATEC	1.41	6.72	0.00	0.00	0.91	1.11
BULL	1.41	1.41	0.00	0.00	0.95	1.05
CRAY	1.41	1.41	0.00	0.00	0.95	1.05
G2_INC	1.41	1.41	0.00	0.00	0.95	1.05
HARRIS	1.41	1.41	0.00	0.00	0.95	1.05
UNISYS	1.41	1.41	0.00	0.00	0.95	1.05
GAZELLE	1.41	1.41	0.00	0.00	0.95	1.05
TRIQUINT	1.41	1.41	0.00	0.00	0.95	1.05
UN_TECHN	1.41	1.41	0.00	0.00	0.95	1.05
Mean	5.01	6.67	2.33	3.21	2.28	3.97
Std	4.80	2.13	4.25	6.48	2.21	3.85
Network Centralisation	13.68	3.06	252.58	30.74	464.04	844.48

In contrast with the RISC network where a few focal firms have an extremely high C_D -value, the distribution of degree based centrality values among companies in the DRAM market is more evenly spread⁴⁴. The degree centrality of Sun Microsystems is 5.9 times the mean and that of MIPS Computer Systems 4.1, while the same ratio is only 3.7 for AMD and Texas Instruments, the two firms with the highest degree centrality in the DRAM network. As a result, it can be argued that the DRAM SA network has a more 'open' character than the RISC network : While 12 firms play a central role in the DRAM network, we have only two or three central players in the RISC case.

Part of this difference can be explained by the different targets of the strategic alliances. In the RISC network, the search for a new industry standard is at the core of most SAs

⁴⁴ The ratio of the mean over the standard deviation is 0.86 for the RISC market and 1.04 for the DRAM market.

such as the licensing of RISC-architectures ; this economic drive implies almost by definition the clustering of firms around a few nodal actors which have a strong grip on the other players. On the contrary, strategic alliances in the DRAM case are to a large extent linked to process technologies and manufacturing capabilities, with R&D joint ventures and cross-licensing for second-sourcing as major SA modes. Such agreements embrace generally no more than two or three partners. The result, is a large but sparse network with a whole range of firms that have only one or two strategic alliances.

The closeness-based centrality index, C_C , shows values are on average much lower than those in the RISC network⁴⁵. The focal firms do not have the same potential for control as in the RISC network. The structure of the network is such that many firms are interconnected with each other, but there is no hub-spoke structure - as in the RISC network - so that some companies have a strong potential for control over the others. The abundance of cycles in the DRAM alliance network implies that most companies can avoid the potential control of another company to which it is linked.

The betweenness centrality of some firms in the DRAM market reach the same level as the three focal companies in the RISC network. Companies as Mitsubishi, AMD, AT&T, LSI-logic, Lucky-Goldstar and SGS-Thomson have a high values for C_B and their value for C_F is even higher with the exception of LSI-Logic. This high values point at strategic alliances that cut across the whole network, improving significantly their centrality in terms of betweenness.

The Bonacich's power based centrality measure shows that no firm in the DRAM market has the same power as MIPS Computer Systems or Sun Microsystems and the mean for both columns is lower than those for the RISC market. A comparison between both columns reveals that a group of American companies (LSI-Logic, Hewlett-Packard, DEC, IBM Intel, and Nat-semiconductor) are powerful partners, but this result is likely to be an artefact of the US Memories consortium.

In short, the DRAM network is much more 'open' than the RISC network. In the latter each firm is linked to a focal partner, which, in turn, have consortia-like agreements with each other about industry standards. In the DRAM network agreements are not exclusive or they imply only a few partners, with the result that many strategic alliances cut across the network. Hence, in RISC network can be divided nicely in three strategic

45 The mean in the RISC network is 2.19 times higher.

blocks⁴⁶. Within each of them relations are abundant but relations across them are scarce because of their exclusivity. The DRAM network is only loosely structured and it is not easy to identify strategic blocks.

This is exactly what we expect from the industry analysis in section 2. The competition between different RISC architectures leads to clearly identifiable strategic groups among which cooperation is excluded (almost) by definition. Most cooperative agreements concerning DRAM chips are process technology based and have no direct relationship with market share competition. Usually, the agreements relate only to two or three companies and they concern frequently multiple distinct spheres of exchange. Therefore, the DRAM network is expected to be a crisscross of SAs without well defined strategic blocks.

4. EVOLUTION OF SA NETWORKS

Strategic alliance networks in high technology evolve relatively fast. The DRAM and RISC networks that have been described in the second section represent the situation at the end of 1989 and differs significantly from the actual situation. As the DRAM network is not directly linked to the competitive success of each firm it is almost impossible to indicate in which direction the network will evolve. But, the situation is different for the RISC network where networking strategies have a direct impact on sales.

The RISC SA network of 1989 seems to contain the seeds of its future evolution and with the hindsight of the most recent years, one can analyze the stability of the RISC network in 1989. The small market shares of the strategic blocks around Sun and MIPS in the workstation and PC market indicate that existing strategic blocks are vulnerable. The dominance of Microsoft is another reason why the cohesion in the strategic blocks supporting UNIX based RISCs could be undermined. More powerful RISCs (e.g. DEC's Alpha) can play a similar role. Finally, as RISCs make inroads in the PC market and other computer segments, incumbents are likely to establish their own SAs, and when they have a large market share in important computer segments, they may have the power to dissolve the existing strategic blocks.

46 'Strategic blocks' are based on similarities in the strategic linkages between companies. See Nohria and Garcia-Pont (1991)

Given the second position of MIPS (see tables) behind Sun, it is not surprising that MIPS spearheaded the formation of the ACE (Advanced Computer Environment) Consortium in 1990 in order to improve its chances. But neither Sun nor MIPS could avoid that their position eroded gradually. The market shares of their strategic blocks in the workstation as well as in the PC market, can be used as an indication of the stability of the network. The growing importance of RISC microprocessors and the poor positions of the SUN- and MIPS-block in the PC market indicate why it was almost inevitable that major PC manufacturers could join forces and eclipse the two early movers.

The most powerful alliance is the PowerPC venture between Apple, IBM, and Motorola : Motorola and IBM combine their RISC microprocessor technology to power Apple's and IBM's computers ranging from notebooks to supercomputers. The combined market share of IBM and Apple in the PC market makes them a serious candidate to establish a new industry standard in the PC market. Motorola seems to win at the expense of Intel who bets on the CISC microprocessors. The PowerPC deal pushes Motorola away from Hewlett-Packard. Therefore, the latter has formed PRO (the Precision RISC Organization) to promote and coordinate the use of its PA-RISC architecture⁴⁷. Beside the PRO it made also agreements with Samsung, Prime Computer and Winbond.

In this way , it is possible to predict the moves of focal players starting from the weakness or instabilities in the current network. This moves will, in turn, trigger strategic action of other players.

5. CONCLUSION

In this paper we argued that our present understanding of cooperative agreements could be substantially improved by taking a network approach instead of using the traditional way of analysing cooperative agreements on a dyadic level or by focusing on the set of SAs of a focal firm. Not only the own SAs but also the structure of the whole SA network determines the competitive position of a firm. Furthermore, the role that SAs play in corporate strategies determine in turn the structure of the network. In order to reveal the differences in network structure and to assess the position of the individual actors in the network we applied a network analysis to two different technologies - RISC microprocessors and DRAM chips - within the micro-electronics industry.

⁴⁷ Some of the founding companies are Convex Computer, Hitachi, Oki, Hughes Aircraft, and Mitsubishi.

Our analysis of both technologies has shown that there exist significant differences between both SA networks, not only in terms of network structure, but also in the role that is played by specific companies in these networks. The network around the RISC technology is clearly structured around two central actors; i.e. MIPS Computer Systems and Sun Microsystems. The DRAM network on the other hand is basically loosely structured. Whereas the network in the RISC market was clearly centered around a few focal actors, the alliances in the DRAM industry were found to be much more evenly spread. Those differences in network structure reflect the differences in the key economic drivers in both set of industries. In this way, industry analysis and network analysis are complementary methods to understand the establishment of SA networks in high-tech industries.

RISC microprocessors are relatively new and are a mounting threat for established industry standards in the PC market. This quest for a new industry standard unleashed the establishment of numerous SAs, as the creation of a *de facto* standard requires support from a large number of other manufacturers. This resulted into a policy of generous licensing of firms with proprietary RISC architectures. Till today, no single RISC architecture has established itself as a new standard and it is unlikely that one ever will on the foreseeable future. To the contrary, firms with proprietary RISC architectures have licensed their technology to develop an 'installed base' in order to obtain a competitive advantage over their rivals. Such licensing agreements creates a strategic block around an architecture. The larger the sales of the strategic block the larger the probability of the architecture to become an industry standard. The aggressive licensing strategy of both companies triggered reactions from the other players with a proprietary RISC design. In the RISC technology, the link between cooperative strategies and market position is a direct one. This contrast with the case of the DRAM chips.

Strategic alliances *vis-à-vis* the DRAM technology are likely to be influenced by the economic features that drive the DRAM process technology such as huge R&D and capital costs, short life cycles and steep learning curves. The escalating R&D and investment costs are one of the main reasons why DRAM manufacturers are teaming up to develop and produce future DRAM generations. Apart from the escalating R&D and investment costs, the DRAM market is also characterized by the rapid succession of different families of DRAMs. The shortness of the production cycle makes dynamic-scale economies important. The DRAM manufacturing process is characterised by significant learning effects, which are the result of improvements in the yield rate. As a result, DRAM manufacturers pursue aggressive pricing policies to be ahead of competitors on

the learning curve. As profits are made during the first year of a new DRAM family, 'time to market' constitutes also an important element for a successful strategy in this industry and is the driving force after the recent international technological cooperative agreements between major DRAM producers. Overall the establishment of agreements that are undertaken in order to lower costs and to speed up leadtimes have led to a network in which a large number of companies are involved.

The centrality measures have shown us that the DRAM network is much more 'open' than the RISC network. In the latter each firm is linked to a focal partners, which, in turn, have consortia-like agreements among each other about industry standards. In the DRAM network agreements are not exclusive or they imply only a few partners, with the result that many strategic alliances cut across the network. As a result, the RISC network can be divided nicely in strategic blocks within each of them relations are abundant but relations across them are scarce because of their exclusivity. The DRAM network is only loosely structured and it is not easy to identify strategic blocks. This differences in network structures is exactly what we expect from the industry analysis. The competition between different RISC architectures and the search for a large customer base leads to clearly identifiable strategic groups. Most cooperative agreements concerning DRAM chips are process technology based and have no direct relationship with market share competition. Therefore the DRAM network is expected to be a crisscross of SAs without well defined strategic blocks.

The various centrality measures have been useful in the analysis of the network structures *vis-à-vis* the two technologies. Differences between the structure of both SA networks reflect the different role SAs play in corporate strategies in both technologies. In this way, industry analysis and network analysis complement each other to understand SA networks better. Of course, centrality measures are only one possible tool to analyse networks and this paper could benefit from additional network methods such as clique detection and structural (or role) equivalence. However, the use of simple centrality measures has already revealed a picture which we would not have been able to capture by analyzing the data on a dyadic level or by analysing the cooperative strategies of a focal firm.

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Annex A: DEFINITIONS OF CENTRALITY MEASURES¹

Point centrality measures

Freeman's (1979) measure of degree centrality (C_D) as the count of number of adjacencies for a point, p_k :

$$C_D(p_k) = \sum_{i=1}^n a(p_i, p_k) \quad (\text{A.1})$$

where $a(p_i, p_k) = 1$ if and only if p_i and p_k are connected by a line, and 0 otherwise.

A relative measure of degree-based point centrality for a given point p_k is defined as follows:

$$C'_D(p_k) = \frac{\sum_{i=1}^n a(p_i, p_k)}{n-1} \quad (\text{A.2})$$

where $n-1$ is the maximum number of points to which a point, p_k , can be connected to.

A closeness-based measure of centrality varies inversely with $d(p_i, p_k)$, the number of edges in the geodesic linking p_i and p_k .

$$C_C(p_k) = \left(1 / \sum_{i=1}^n d(p_i, p_k) \right) \quad (\text{A.3})$$

However, C_C is only meaningful for a connected graph. In a unconnected graph every point is at infinite distance from at least one other point. Relative centrality of point p_k can be defined as:

$$C'_C(p_k) = \left((n-1) / \sum_{i=1}^n d(p_i, p_k) \right) \quad (\text{A.4})$$

The betweenness-based centrality can be measured as follows:

$$C_B(p_k) = \sum_i^n \sum_{j < k}^n \frac{g_{ij}(p_k)}{g_{ij}} \quad (\text{A.5})$$

¹ For a more detailed discussion of centrality measures, we refer the reader to Bonacich (1987), Freeman(1979), Freeman *et al.* (1991), and Gould (1987).

where n is the number of points in the graph, g_{ij} the number of geodesics linking p_i and p_j and $g_{ij}(p_k)$ is the number of geodesics linking p_i and p_j that contain p_k . The relative measure of betweenness centrality is :

$$C'_B(p_k) = \left(2 \sum_i^n \sum_{j < i}^n \frac{g_{ij}(p_k)}{g_{ij}} / (n^2 - 3n + 2) \right) \quad (A.6)$$

A centrality measure for valued graphs based on the maximum amount of information flow between two points was developed by Freeman *et al.* (1991). Let m_{ij} be the maximum flow from a point p_i to another p_j . And let $m_{ij}(p_k)$ be the maximum flow from p_i to p_j that passes through point p_k . Then the degree to which the maximum flow between all unordered pairs of points depends on p_k , where $i < j$ and $i \neq j \neq k$ is

$$C_F(p_k) = \sum_i^n \sum_{j < i}^n m_{ij}(p_k) \quad (A.7)$$

If the previous formula is divided by the total flow between all pairs of points where p_k is neither a source nor a sink, we can define a relative measure of flow betweenness as follows:

$$C'_F(p_k) = \frac{\sum_i^n \sum_{j < i}^n m_{ij}(p_k)}{\sum_i^n \sum_{j < i}^n m_{ij}} \quad (A.8)$$

Connected graphs without cycles have only one path - a single geodesic - linking any pair of points and have as a consequence the same values for C_B and C_F . When cycles are presents these two centrality measures will differ because C_B measures record flow only along the geodesics, while the C_F measures are responsive to all paths along which information can flow.

Finally, we calculated also point centralities based on Bonacich's power index (1987). Consider an adjacency matrix A_{ij} , the centrality if point i , $c(p_i)$, is given by:

$$c(p_i) = \sum_j (\alpha + \beta \cdot c(p_j)) \cdot A_{ij} \quad (A.9)$$

The value of α is used to normalise the measure, the value of β is an attenuation factor which reflects the the amount of dependence of each point's centrality on the centralities of the points it is adjacent to. The normalization parameter, α , is selected so that the sum of the squares of the point centralities is the size of the network.

If $\beta=0$, the Bonacich's power based centrality measure calculates directly proportional to the degree of each points. If $\beta>0$, then more weight is given to being connected to powerful actors. Negative values for β give more weight to being connected to low powered actors.

Graph centrality measures

When the notion "centrality" is applied to whole networks, it refers to differences in point centrality. If n is the number of points, $C_X(p_i)$ one of the point centralities defined above, and $C_X(p^*)$ the largest of $C_X(p_i)$ for any point in the network, then :

$$C_X = \frac{\sum_{i=1}^n (C_X(p^*) - C_X(p_i))}{\max \sum_{i=1}^n (C_X(p^*) - C_X(p_i))} \quad (A.10)$$

is Freeman's (1979) index for graph centrality. The denominator represents the maximum possible sum of differences in point centrality for a graph with n points. This maximum usually coincides with the point centrality of a star.

When (A.10) is applied to the point centralities as we have them defined above, we get the following formulas for network centrality.

The degree based network centrality measure,

$$C_D = \frac{\sum_{i=1}^n (C_D(p^*) - C_D(p_i))}{n^2 - 3n + 2} \quad (A.11)$$

the closeness based centrality measure,

$$C_C = \frac{\sum_{i=1}^n (C_C(p^*) - C_C(p_i))}{(n^2 - 3n + 2)/(2n - 3)} \quad (\text{A.12})$$

the one based on betweenness,

$$C_B = \frac{\sum_{i=1}^n (C_B(p^*) - C_B(p_i))}{n^3 - 4n^2 + 5n - 2} \quad (\text{A.13})$$

and the flow betweenness centrality measure.

$$C_F = \frac{\sum_{i=1}^n (C_F(p^*) - C_F(p_i))}{n - 1} \quad (\text{A.14})$$

The power network centralisation index is:

$$C_P = \sum_i (c(p^*) - c(p_i)) / (n - 1) \quad (\text{A.15})$$

where $c(p_i)$ represents the point centrality as defined in (A.9).

Annex B : RISC chips and manufacturing firms

Company	Architecture	Chip	Manufacturers
Hewlett-Packard Co. (US)	PA	PA-4 PA-7100	Hitachi (J) Samsung (SK) HP (US) (captive) Oki (J) Mitsubishi (J)(captive) Winbond (Taiwan)
Intel Corp.(US)	i860	860XP	Intel (US)
Apple/IBM/ Motorola (US)	Power PC	Power PC 601	IBM (US) Motorola (US)
Motorola	88000		Motorola (US)
MIPS Computer Systems (US)		R3000 R4000 R4400	IDT (US) Q.E.D. (US) LSI Logic (US) Performance Semicond. US) Siemens (G) NEC (J) BIT (US) Sony (J) Toshiba (J) Macronix (Taiwan)
Sun Microsystems (US)	SPARC	HyperSPARC Viking SuperSPARC microSPARC	Cypress (US) Fujitsu (J) LSI Logic (US) TI (US) TI (US) Philips (NL) Matsushita (J)(captive) Toshiba (J) (captive) Weitek (US) DEC (US) Cypress (US) Samsung (SK) Motorola (US) (foundry) Fujitsu (J) (foundry) Sanyo (J)
DEC Corp. (US)	Alpha		VLSI Technology (US) GEC Plessey (UK)
Intergraph (US)	Clipper		Hitachi (J) NEC (J)
Acorn Computers (US)	ARM	ARM60	Nat. Semic. (US)
AT&T (US)	Hobbit		
National Semic. (US)	Swordfish		

Sources: IEEE Spectrum (April 1991, p.61)
 IEEE Spectrum (July 1992, p. 28)
 ICE (1992, p. 6-33)
 ICE (1993, p. 6-34)

Annex C : Representative sample of commercially available workstations in the U.S.A. in 1991

Central processing unit		Workstation manufacturer
CISC		
Cypress	Cypress CY7C601	Mars Microsystems Inc. Solarix Systems Star Technologies Inc. EE International omputer Corp. Mars Microsystems Inc. Acer America Corp. American Mitac Corp. Arche Technologies Inc. AT&T Computer Systems Compaq Computer Corp. Copam USA Inc. Dell Computer Corp. Dolch Computer Systems EE International Computer Corp. Fortron/Source Corp. Laser Digital Inc. Microway Inc. Micro Express Mobius Computer Corp. NCR Corp. Polywell Computers Inc. Tangent Computer Inc. TeleCAD TeleVideo Systems Inc. Wyse Technology Inc.
SGS-Thomson	Inmos T800	Apple Computer Inc.
Intel	Intel 80386	Commodore Business Machines Inc.
	Intel 80486	Concurrent Computer Corp. Hewlett-Packard Co.
Motorola	Motorola 68030	
	Motorola 68040	
RISC		
	Custom	International Business Machines Corp.
	Custom	Visual Information Technologies Inc.
Intel	Intel i860	EE International Computer Corp.
Intergraph	Intergraph C300	Intergraph Corp.
LSI Logic	LSI Logic Sparkit 20	CompuAdd Corp.
	LSI Logic 64801	Tatung Science and Technology Inc.
	LSI Logic L64084	Twinhead International Corp.
MIPS	MIPS R3000	Control Data Corp. Digital Equipment Corp. Evans & Sutherland Design Systems Division MIPS Computer Systems Inc. Silicon Graphics Inc. Sony Microsystems Co. Stardent Computer Inc. Solbourne Computer Inc. Ramtek Corp. RDI Inc. Sun Microsystems Inc.
Sun	Panasonic MN 10501	
	Sparc Engine	
	Sun Sparc	

Source: Adapted from IEEE Spectrum, April 1991, pp. 40-46.

Annex D: COMPANIES INCLUDED IN THE RISC AND DRAM SA NETWORK

DRAM NETWORK

	Name	Code	Country
1	Acer	ACER	TAIWAN
2	Advanced Micro Devices Inc.	AMD	USA
3	American Telephone & Telegraph Co.	AT&T	USA
4	Amstrad Plc.	AMSTRAD	UK
5	Applied Micro Systems Corp.	APPMICRS	USA
6	Groupe Bull	BULL	FRANCE
7	Chips and Technologies	CHIPS_T	USA
8	Commodore	COMMODORE	USA
9	Cray Research Inc.	CRAY	USA
10	Cross & Trecker Corp.	CROSS_TR	USA
11	Cypress Semiconductor	CYPRESS	USA
12	Dell Computer	DELLCOMP	USA
13	Docas	DOCAS	BRA
14	Erso	ERSO	ROC
15	Exel microelectronics	EXEL_MIC	USA
16	Force Computers Inc.	FORCE_C	USA
17	Fujitsu Ltd.	FUJITSU	JAPAN
18	Fuyo Group	FUYO	JAPAN
19	Digital Equipment Corp.(DEC)	DEC	USA
20	Formosa Plastic Corp.	FORMOS_P	USA
21	Gazelle microcircuits	GAZELLE	USA
22	General Electric	GE	USA
23	General Electric Company	GEC	UK
24	G-2 Inc.	G2_INC	USA
25	Harris Corp.	HARRIS	USA
26	Hewlett-Packard Co.	H-P	USA
27	Hitachi Ltd.	HITACHI	JAPAN
28	Hyundai	HYUNDAI	S-KOREA
29	Int. CMOS Technology	INT_CT	USA
30	Integrated Device Technology	INTEG-DT	USA
31	International Business Machines	IBM	USA
32	Intel Corp.	INTEL	USA
33	Itan	ITAN	BRA
34	Kaypro Corp.	KAYPRO	USA
35	LSI Logic	LSILOGIC	USA
36	Lucky Goldstar Ltd.	LUCKY-G	S-KOREA
37	Matra MHS	MATRA_MHS	FRANCE
38	Matsushita Elect.Industrial Co.Ltd.	MATSUSHT	JAPAN
39	Micron Technology Inc.	MICRON_T	USA
40	Mitsubishi Electric Corp.	MITSUBIS	JAPAN
41	Motorola Inc.	MOTOROLA	USA
42	National Cash Register Corp.(NCR)	NCR	USA
43	National Semiconductor Corp.	NAT_SEMI	USA
44	NEC Corp.	NEC	JAPAN
45	NMB Semiconductor	NMB	JAPAN
46	Nitron	NITRON	USA
47	NTT	NTT	JAPAN
48	Olivetti SpA.	OLIVETTI	ITALY
49	Panatec R&D Corp.	PANATEC	USA
50	Paradigm Technologies Inc.	PARADIGM	USA
51	Philips N.V.	PHILIPS	NETHERLANDS
52	Ricoh	RICOH	JAPAN
53	Sagem	SAGEM	FRA
54	Samsung	SAMSUNG	S-KOREA
55	Schlumberger N.V.	SCHLUMB	USA
56	Sharp	SHARP	JAPAN
57	Siemens A.G.	SIEMENS	GERMANY
58	Sony	SONY	JAPAN
59	STC	STC	UK
60	Tandy	TANDY	USA
61	Texas Instruments Inc.	TI	USA

62	Thomson S.A. (SGS-Thomson)	THOMSON	FRANCE/ITALY
63	Toshiba Corp.	TOSHIBA	JAPAN
64	Triquint	TRIQUINT	USA
65	Unisys Corp.	UNISYS	USA
66	Universal Semiconductor	UNI_SEMI	USA
67	United Technologies Corp. (UTV)	UN_TECHN	USA
68	VLSI Technology Inc.	VLSI	USA
69	Westinghouse	WESTINGH	USA
70	Wyse	WYSE	USA
71	Xerox Corp.	XEROX	USA
72	Xicor	XICOR	USA
73	Xylogics	XYLOGICS	USA

RISC NETWORK

	Name	Code	Country
1	Advanced Micro Devices Inc.	AMD	USA
2	American Telephone & Telegraph Co.	AT&T	USA
3	Apollo Computer	APOLLO	USA
4	Arete Systems Corp.	ARETE	USA
5	Bipolar Integrated Technology	BIPOLAR	USA
6	Control Data Corp.	CDC	USA
7	Cypress Semiconductor	CYPRESS	USA
8	Fujitsu Ltd.	FUJITSU	JAPAN
9	Data General Corp.	DATA-GEN	USA
10	Digital Equipment Corp.(DEC)	DEC	USA
11	Hewlett-Packard Co.	H-P	USA
12	Hitachi Ltd.	HITACHI	JAPAN
13	Integrated Device Technology	INTEG-DT	USA
14	Intergraph	INTERGRA	USA
15	Kubota Corp.	KUBOTA	JAPAN
16	LSI Logic	LSILOGIC	USA
17	Lucky Goldstar Ltd.	LUCKY-G	S-KOREA
18	Matsushita Elect.Industrial Co.Ltd.	MATSUSHT	JAPAN
19	Metaflow Technologies	METAFLOW	USA
20	Mips Computer Systems	MIPS-CS	USA
21	Motorola Inc.	MOTOROLA	USA
22	National Cash Register Corp.(NCR)	NCR	USA
23	Olivetti SpA.	OLIVETTI	ITALY
24	Performance Semiconductor	PERF-SEM	USA
25	Philips N.V.	PHILIPS	NETHERLANDS
26	Prime Computer Inc.	PRIME	USA
27	Racal	RACAL	UK
28	Schlumberger N.V.	SCHLUMB	USA
29	Siemens A.G.	SIEMENS	GERMANY
30	Silicon Graphics	SILICONG	USA
31	Stardent Inc.	STARDENT	USA
32	Sté.de Dév.Ind.de Matériel & d'Ass.	SODIMA	FRANCE
33	NEC Corp.	NEC	JAPAN
34	Sun Microsystems	SUN-MICR	USA
35	Tandem Computers Corp.	TANDEM	USA
36	Tektronix Inc.	TEKTRONX	USA
37	Texas Instruments Inc.	TI	USA
38	Thomson S.A. (SGS-Thomson)	THOMSON	FRANCE/ITALY
39	Toshiba Corp.	TOSHIBA	JAPAN
40	UniSoft	UNISOFT	UK
41	Unisys Corp.	UNISYS	USA
42	VLSI Technology Inc.	VLSI	USA
43	Xerox Corp.	XEROX	USA